

EXAMINER'S AMENDMENT

1. Claims 3-22, and 32 are pending in the instant application.
2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Andrew T. Harry on October 9, 2008.

The application has been amended as follows wherein the following versions of claims 4, 6-8, 10, 12, and 16 replace all prior versions in their entirety:

Claim 4: The system according to Claim 10, wherein

said ~~transmission node comprises a~~ data clock transmitter configured to ~~transmit~~ further transmits a data clock to said receiving node via said link, said data clock defining ~~said a~~ timing of said data elements or components of said data elements, and

said reception node comprises a data clock receiver configured to receive said data clock from said transmitting node and output said data elements in accordance with said received data clock.

Claim 6: The system according to claim 4, wherein:

said transmission node comprises a combiner configured to combine said synchronization clocking signal and said data clock to form a multiplexed clock signal for transmission to said reception node via said link; and

said ~~reception node~~ data clock receiver comprises a demultiplexer configured to demultiplex said synchronization clocking signal and said data clock from said multiplexed clock signal.

Claim 7: The system according to claim 6, wherein said combiner comprises a timing adjuster configured to adjust the timing of a subset of clock pulses of said data clock signal in dependence on a said synchronizing feature of said synchronization clocking signal.

Claim 8: The system according to claim 7, wherein:

said data clock is defined with respect to a periodic reference clock ~~edge~~ edges;

said transmission node is configured to adjust the timing of one or more clock edges of said data clock other than the periodic reference edges in response to a said synchronizing feature of said synchronization clocking signal; and

said reception node comprises a timing deviation detector configured to detect timing deviations in clock edges of said data clock other than the periodic reference edges.

Claim 10: A data communications system for communicating a data signal formed of successive data elements, said system comprising a transmission node, a reception node, and a link providing a data connection from said transmission node to said reception node,

said transmission node comprising:

a ~~clocking-signal~~ data clock transmitter configured to transmit a synchronization clocking signal to said reception node via said link, said synchronization clocking signal having synchronizing features occurring at a frequency lower than a data element rate; and

an assembler configured to assemble elements of said data signal into data frames, each data frame having a plurality of successive data elements of said data signal, for transmission to said reception node via said link, said assembler being responsive to said synchronization clocking signal so as to set a synchronization flag associated with a data element having a first predetermined temporal relationship with a synchronizing feature of said synchronization clocking signal; and

said reception node comprising:

a detector configured to detect a said synchronizing feature of said synchronization clocking signal received from said transmission node;

a disassembler configured to disassemble received data frames to regenerate said data signal, said disassembler being operable to detect a data element associated with a said set synchronization flag; and

an output unit configured to output a said data element associated with a said set synchronization flag at a second predetermined temporal

Art Unit: 2611

relationship with respect to said synchronizing feature of said received synchronization clocking signal, said output unit comprising a time delay arrangement, so that data elements from a data frame associated with a said set synchronization flag are output a predetermined delay time after said reception node receives said synchronizing feature of said synchronization clocking signal,

wherein said first and second predetermined temporal relationships are arranged so that a predetermined system latency exists between input of a data element to said transmission node and subsequent output of that data element by said reception node.

Claim 12: A data communications system for communicating a data signal formed of successive data elements, said system comprising a transmission node, a reception node, and a link providing a data connection from said transmission node to said reception node,

said transmission node comprising:

a ~~clocking signal~~ data clock transmitter configured to transmit a synchronization clocking signal to said reception node via said link, said synchronization clocking signal having synchronizing features occurring at a frequency lower than a data element rate; and

an assembler configured to assemble elements of said data signal into data frames, each data frame having a plurality of successive data elements of said data signal, for transmission to said reception node via said link, said assembler being responsive to said synchronization clocking signal so as to set a synchronization flag associated with a data element having a first predetermined

temporal relationship with a synchronizing feature of said synchronization clocking signal, said assembler comprising a frame assembly arrangement configured to receive input data elements at an input data rate and to buffer the input data elements prior to performing a frame assembly operation in which buffered data is retrieved and assembled to form the framed data, said frame assembly arrangement configured to output said framed data for transmission at a framed data rate; and

said reception node comprising:

a detector configured to detect a said synchronizing feature of said synchronization clocking signal received from said transmission node;

a disassembler comprising a frame receiving arrangement configured to receive framed data from said transmission node at said framed data rate and to buffer said received framed data, and to disassemble said buffered received frame data to regenerate said data signal, said disassembler configured to detect a data element associated with a said set synchronization flag; and

an output unit configured to output a said data element associated with a said set synchronization flag at a second predetermined temporal relationship with respect to said synchronizing feature of said received synchronization clocking signal,

wherein said first and second predetermined temporal relationships are arranged so that a predetermined system latency exists between an input of a data element to said transmission node and a subsequent output of ~~that~~ such data element by said reception node, and output of framed data is commenced

Art Unit: 2611

by said frame assembly arrangement prior to assembly of a complete frame and output of data blocks is commenced by said frame receiving arrangement prior to disassembly of a complete frame of received framed data.

Claim 16: The system according to claim 15, wherein said data elements are derived from Audio Engineering Standard 3 (AES3) ~~AES3 standard~~ audio sample subframes.

Claim 10 is renumbered as claim 1, claims 3-9, 11, 13-22, and 32 are renumbered respectively as claims 2-20, claim 12 is renumbered as claim 21, and the claim dependency is renumbered accordingly.

Allowable Subject Matter

3. Claims 3-22, and 32 renumbered as claims 1-21 are allowed.

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to JASON M. PERILLA whose telephone number is (571)272-3055. The examiner can normally be reached on M-F 8-5 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh M. Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2611

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jason M Perilla/
Primary Examiner, Art Unit 2611
October 9, 2008

/jmp/

/Chieh M Fan/
Supervisory Patent Examiner, Art Unit 2611